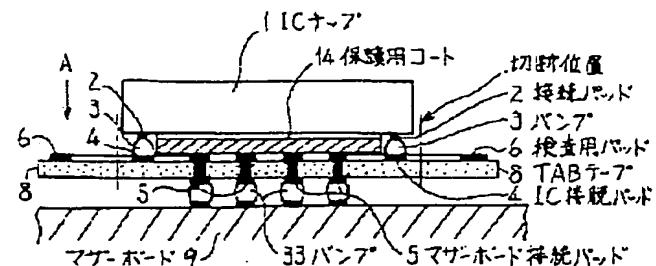
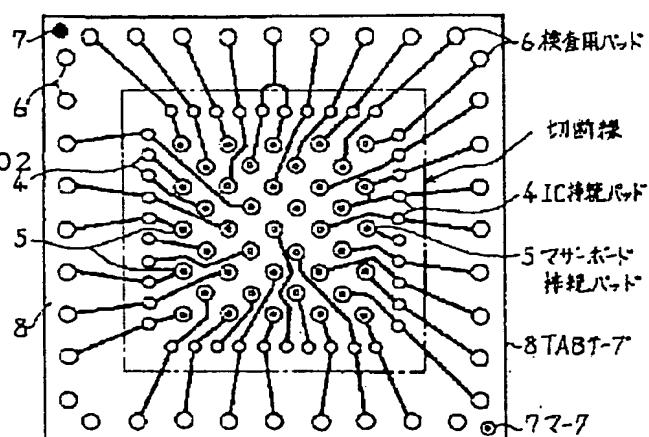


(a) 前面図



(b) TABテープのA観図



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PATENTEE : FUJITSU LTD

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INVENTOR : NOKIMURA HITOSHI; others: 02

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TITLE : TAB MOUNTING STRUCTURE FOR
INTEGRATED CIRCUIT USE

ABSTRACT : PURPOSE: To provide a TAB mounting structure for integrated circuit use, wherein an IC chip is mounted on a mother board, a check on the element of the chip and a check subsequent to a connection of the element of the chip can be performed, a reduction in a mounting area and a multiterminal structure for connection are contrived and a die bonding is not permitted to perform.

CONSTITUTION: The title TAB mounting structure is constituted of an IC chip 1 with all connection pads 2 arranged on its one surface, IC connection pads 4, on which the chip 1 is mounted in a face down manner and which are welded and connected to the pads 2 via bumps 3 and are provided at positions opposed to the chip 1, mother board connection pads 5, which are made to have continuity with the respective pads 4 through the opposite surfaces to their surfaces, are made to weld and connect to a mother board 9 via bumps 33 and are provided within roughly the projected area of the chip 1, pads 6 for inspection use, which are connected to pads 4 of a desired circuit and are provided at positions on the outer periphery of a TAB tape 8, and the TAB tape 8, which is provided with masks 7 for performing an alignment of the connection of the tape 8 with the board 9 on its peripheral edge parts and has conductors formed by patterning on both surfaces or in a multilayer.